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CLAIMS

What is claimed is:

1. A method comprising:

identifying a plurality of ports available in a plurality of interface cards in a device; and

selecting a grouping of ports of the plurality of ports as a Multi-Link Trunk (MLT), at least one port of the grouping of ports is located in an interface card separate from another port of the grouping of ports which is located in another interface card.

2. The method of claim 1, wherein the grouping of ports includes at least two of the plurality of ports.

3. The method of claim 2, further comprising:

storing the identified plurality of ports in a memory.

4. The method of claim 2, further comprising:

determining if a port included in the MLT has failed;

selecting another port from the identified plurality of ports; and

replacing the failed port with the selected port.

5. The method of claim 2, further comprising:

determining if a bandwidth can be channeled by the MLT;

if the bandwidth cannot be channeled by said MLT, then

selecting one or more ports from the identified plurality of ports;

adding the one or more ports to the MLT until the MLT can channel the bandwidth.

6. The method of claim 2, wherein selecting the grouping of ports further comprises selecting the ports that are secure.

7. An apparatus comprising:

a first circuit to identify a plurality of ports available in a plurality of interface cards in a device; and

a second circuit to select a grouping of ports of the plurality of ports as a Multi-Link Trunk (MLT), at least one port of the grouping of ports is located in an interface card separate from another port of the grouping of ports which is located in another interface card.

8. The apparatus of claim 7, further comprising:

a memory to store the identified plurality of ports.

9. The apparatus of claim 7, further comprising:

a third circuit to determine if a port included in an MLT has failed;

a fourth circuit to select another port from the identified plurality of ports; and

a fifth circuit to replace the failed port with the selected port.

10. The apparatus of claim 7, further comprising:

a seventh circuit to determine if a bandwidth can be channeled by the MLT;

an eighth circuit to select one or more ports from the identified plurality of ports if the bandwidth cannot be channeled by the MLT; and

a ninth circuit to add the one or more ports to the MLT until the MLT can channel the bandwidth.

11. The apparatus of claim 7, further comprising a tenth circuit to select the grouping of ports that are secure.

12. A processor readable medium which when executed by a processor causes the processor to perform a method comprising:

identifying a plurality of ports available in a plurality of interface cards in a device; and

selecting a grouping of ports of the plurality of ports as a Multi-Link Trunk (MLT), at least one port of the grouping of ports is located in an interface card separate from another port of the grouping of ports which is located in another interface card.

13. The processor readable medium of claim 12, further comprising:

storing the identified plurality of ports in a memory.

14. The processor readable medium of claim 12, further comprising:

determining if a port included in an MLT has failed;

selecting another port from the identified plurality of ports; and

replacing the failed port with the selected port.

15. The processor readable medium of claim 12, further comprising:

determining if a bandwidth can be channeled by said MLT;

if the bandwidth cannot be channeled by the MLT, then

selecting one or more ports from the identified plurality of ports;

adding the one or more ports to the MLT until the MLT can channel the bandwidth.

16. The processor readable medium of claim 12, wherein selecting a grouping of ports further comprises selecting the ports which are secure.

17. An apparatus comprising:

a first memory to store a plurality of port addresses, of which a grouping of the port addresses is selected for Multi-Link Trunk (MLT);

a port selector circuit coupled to the first memory, the port selector circuit to transmit a first signal to the first memory;

a load sharing circuit coupled to the first memory, the load sharing circuit to transmit a second signal to the first memory, the second signal and the first signal index a port address in the first memory and the indexed port address addresses a port selected to transmit data.

18. The apparatus of claim 17, wherein the first signal of the port selector circuit indexes the grouping of port addresses belonging to the MLT and the second signal of the load sharing circuit indexes one of the port addresses in the MLT indexed by the port selector circuit.

19. The apparatus of claim 17, wherein the load sharing circuit further comprises:

an identification circuit to generate an identification for the data to be transmitted; and

an identification indexing circuit to place the identification in one of a plurality of indices, wherein each index has a corresponding physical port in the MLT.

20. The apparatus of claim 19, wherein the identification circuit includes a random generator that assigns the identification to the data.

21. The apparatus of claim 20, wherein the random generator further comprises a first circuit to randomly generate the identification based on at least a portion of one of a source address of the data, a destination address of the data, and both the source address and the destination address of the data.

22. The apparatus of claim 21, wherein the first circuit is a plurality of Exclusive - OR (XOR) gates.

23. The apparatus of claim 19, wherein the identification indexing circuit includes a second memory to store a modulus (MOD) function table wherein a base of the MOD function is determined by a number of active ports of the MLT and the MOD function is performed on the identification using the MOD function table and a result of the MOD function is used as the index.

24. The apparatus of claim 23 wherein the physical port selector circuit comprises:

a third memory to store a plurality of MLTs, each of the MLTs having a grouping of port addresses identified in the first memory;

a fourth memory to store a plurality of numbers of active ports, wherein each stored number of active ports correspond to an MLT stored in the third memory; and

a second circuit configured to select a port address in the first memory using an identified MLT in the third memory and the index generated by the load sharing circuit.

25. A method comprising:

identifying a Multi-Link Trunk (MLT) in which data is to be transmitted;

identifying a plurality of ports included in the MLT;

generating an identification for the data to be transmitted; and

using the identification to determine a port in which the data is to be transmitted in the MLT.

26. The method of claim 25, wherein generating the identification further comprises:

generating the identification using a random generator.

27. The method of claim 26, further comprising:

selecting a portion of at least a source address and/or a destination address of the data on which Exclusive - OR (XOR) operation is performed to generate the identification.

28. The method of claim 26, wherein using the identification to determine a physical port further comprises:

determining a number of ports in the MLT;

using the number of ports as a base for a modulus (MOD) function;

performing the MOD functions on the identification; and

using a result of the MOD function as an index to select one of the ports in said MLT.

29. A processor readable medium which when executed by a processor causes the processor to perform a method comprising:

identifying a Multi-Link Trunk (MLT) in which data is to be transmitted;

identifying a plurality of ports included in the MLT;

generating an identification for the data to be transmitted; and

using the identification to determine a physical port in which the data is to be transmitted in the MLT.

30. A processor readable medium as in claim 29, wherein generating the identification further comprises:

generating the identification using a random generator.

31. The processor readable medium of claim 29, further comprising:

selecting a portion of at least a source address and/or a destination address of the data on which Exclusive-OR (XOR) function is performed to generate the identification.

32. The processor readable medium of claim 29, wherein using the identification to determine a port further comprises:

determining a number of ports in the MLT;

using the number of ports as a base for a modulus (MOD) function;

performing the MOD function on the identification; and

using a result of the MOD function as an index to select one of the ports in the MLT.

33. An apparatus comprising:

a first memory to store a plurality of Multicast Group Identification (MGID), each MGID identifies a plurality of ports;

a load sharing circuit to transmit a first signal to the first memory;

an MGID selector circuit to transmit a second signal to the first memory, the first signal and the second signal selects an MGID which identifies a plurality of ports in which data is multicasted.

34. The apparatus of claim 33, wherein the load sharing circuit further comprises:

an identification circuit to generate an identification for the data to be multicasted; and

an identification indexing circuit to place the identification in one of a plurality of indices, wherein each index has a corresponding MGID.

35. The apparatus of claim 34, wherein the identification circuit includes a random generator that assigns the identification to the data.

36. The apparatus of claim 35, wherein the random generator further comprises:

a first circuit randomly generate the identification based on at least a portion of one of a source address of the data, a destination address of the data, and both the source address and the destination address of the data.

37. The apparatus of claim 36, wherein the first circuit is a plurality of Exclusive - OR (XOR) gates.

38. The apparatus of claim 34, further comprising:

a second memory to store a plurality of master MGIDs, each master MGID identifying a plurality of MGIDs;

the identification indexing circuit includes,

a third memory to store a modulus (MOD) function table wherein a base of the MOD function is determined by to a highest number of physical ports in any Multi-Link Trunk (MLT) in the plurality of MGIDs identified by a master MGID, and a MOD operation is performed on the identification using the MOD function table and a result of the MOD function is used as the index.

39. The apparatus of claim 38, wherein the MGID port selector circuit comprises:

a second circuit configured to select the MGID in the first memory using an identified master MGID from the second memory and the index generated by the load sharing circuit.

40. The apparatus of claim 33, further comprising a third circuit configured to select an MGID of a port in which data is received as the MGID, which identifies the plurality of physical ports in which data is to be multicasted, if the receiving port is a port in a Multi-Link Trunk (MLT).

41. A method comprising:

assigning at least one Multicast Group Identification (MGID) to a physical port to be used for multicasting in a multicast domain;

determining whether a data receiving port is a physical port in a Multi-Link Trunk (MLT) or a non-MLT port;

if the receiving port is the physical port in the MLT, then assigning an MGID of the receiving port as the multicast domain MGID which identifies a plurality of physical ports to multicast the data.

42. The method of claim 41, further comprising:

if the receiving port is the non-MLT port, then

determining a master MGID that is assigned to the multicast domain;

determining a plurality of MGIDs identified by the master MGID;

obtaining an identification for the received data; and

using the identification to determine an MGID in the plurality of MGIDs which identifies a plurality of physical ports to multicast the data.

43. The method of claim 41, further comprising:

determining a highest number of physical ports in any MLT in a plurality of MGIDs identified by the master MGID;

using the highest number of physical ports as base for a modulus (MOD) function;

performing a MOD function on the identification; and

using a result of the MOD function as an index to determine one of the MGIDs identified by the master MGID as the MGID identifying a plurality of physical ports to multicast the data.

44. The method of claim 42, wherein obtaining the identification includes selecting a portion of at least a source address and/or a destination address of the data on which Exclusive - OR (XOR) function is performed to generate the identification.

45. A processor readable medium which when executed by a processor causes the processor to perform a method comprising:

assigning at least one Multicast Group Identification (MGID) to a physical port to be used for multicasting in a multicast domain;

determining whether a data receiving port is a physical port in a Multi-Link Trunk (MLT) or a non-MLT port;

if the receiving port is the physical port in the MLT, then assigning an MGID of said receiving port as said multicast domain MGID which identifies a plurality of physical ports to multicast the data.

46. The processor readable medium of claim 43, further comprising:

if the receiving port is the non-MLT port, then

determining a master MGID that is assigned to the multicast domain;

determining a plurality of MGIDs identified by the master MGID;

obtaining an identification for said received data; and

using the identification to determine an MGID in the plurality of MGIDs which identifies a plurality of physical ports to multicast the data.

47. The processor readable medium of claim 44, further comprising:

determining a highest number of physical ports in any MLT in a plurality of MGIDs identified by the master MGID;

using the highest number of physical ports as base for a modulus (MOD) function;

performing a MOD function on the identification; and

using a result of the MOD function as an index to determine one of the MGIDs identified by the master MGID as the MGID identifying a plurality of physical ports to multicast the data.

48. A processor readable medium of claim 46, wherein obtaining the identification includes selecting a portion of at least a source address and/or a destination address of the data on which are Exclusive -OR (XOR) function is performed to generate the identification.